

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of:

APPLICANTS: Hiroyuki MIZUNO et al.  
SERIAL NO.: To be assigned  
FILED: Herewith  
FOR: SEMICONDUCTOR INTEGRATED CIRCUIT  
GROUP ART UNIT: 2816 (anticipated)  
EXAMINER: Jeffrey S. Zweizig (anticipated)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to deposit account 11-0600.

1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on

the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

- a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).
- b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).
- c. Please debit Deposit Account No. 11-0600 in the amount of \$180.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 CFR §1.97(c)(2).

3. This Information Disclosure Statement is being filed after the mailing date of a final action, Notice of Allowance or an action that otherwise closes prosecution, but before payment of the Issue Fee. Applicant(s) hereby request(s) that the Information Disclosure Statement be considered. Please debit Deposit Account No. 11-0600 in the amount of \$180.00 in payment of the petition fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

- a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in any counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).
- b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

4. Relevance of the non-English language reference(s) is discussed in the present specification.

5. The reference(s) was/were cited in a counterpart foreign application. An English language version of the foreign search report is attached for the Examiner's information.

6. A concise explanation of the relevance of the non-English language reference(s) appears in the Appendix attached hereto.

7. The Examiner's attention is directed to co-pending U.S. Patent Application No. \_\_\_\_\_, filed, which is directed to related technical subject matter. The identification of this U.S. Patent Application is not to be construed as a waiver of secrecy as to that application now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited application and the art cited therein during examination of the present application.

8. This application is one of a series of related applications, identified in the attached Appendix, which are directed to related technical subject matter. The identification of those U.S. Patent Applications is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during the examination.

9. The reference(s) was/were cited by or submitted to the Office in parent application numbers 09/582,485 and 10/443,018, which is relied upon for an earlier filing date under 35 U.S.C. §120. Thus, copies of these references are not attached. 37 CFR §1.98(d).

10. English-language Abstracts of the non-English language references are attached hereto.

11. Since this application was filed after June 30, 2003, copies of U.S. references are not included.

12. Other.

Respectfully submitted,

KENYON & KENYON

  
David J. Zibelli  
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Date: January 29, 2004

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**FORM PTO-1449****INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT(S)**

Atty Docket No.: 29287/141  
 Serial No.: To be assigned  
 Inventors: Hiroyuki MIZUNO et al.  
 Filed: January 29, 2004  
 Group Art Unit: 2816 (anticipated)  
 Examiner: J.S. Zweizig (anticipated)

**U.S. PATENT DOCUMENTS**

<u>Examiner Initial</u>	<u>Patent Number</u>	<u>Patent Date</u>	<u>Name</u>	<u>Class/Subclass</u>	<u>Filing Date</u>
	6,380,798	04-2002	MIZUNO et al.	327/534	
	6,337,593	01-2002	MIZUNO et al.	327/534	
	6,292,015	09-2001	OOISHI et al.	326/33	
	6,191,615	Feb. 2001	KOGA	326/81	
	6,177,831	Jan. 2001	YONEDA et al.	327/537	
	6,097,113	Aug. 2000	TERAOKA et al.	307/125	
	6,046,627	04-2000	ITOH et al.	327/546	
	5,786,724	Jul. 1998	TEGGATZ	327/534	
	5,659,517	08/19/97	ARIMOTO et al.	365/226	
	5,610,533	Mar. 1997	ARIMOTO et al.	326/33	
	5,721,510	02-1998	MIYAJIMA	327/536	
	4,628,215	12/09/86	LOU	307/200	

**FOREIGN PATENT DOCUMENTS**

<u>Examiner Initial</u>	<u>Document Number</u>	<u>Date</u>	<u>Country</u>	<u>Class/Subclass</u>	<u>Translation Yes</u>	<u>No</u>
	JP7-254685	10/3/95	Japan			
	JP8-83487	3/26/96	Japan			
	JP8-204140	8/09/96	Japan			
	06-053496	02/25/94	Japan			
	60-020550	02/01/85	Japan			
	01-098254	04/17/89	Japan			
	08-249882	09/27/96	Japan			
	01-318261	12/22/89	Japan			
	04-345061	12/01/92	Japan			
	05-190672	07/30/93	Japan			
	02-154446	06/13/90	Japan			

EXAMINER

DATE CONSIDERED

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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**OTHER DOCUMENTS**  
(Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner  
Initial

- \_\_\_\_\_ 1. Kiyoo Ito, "VLSI Memory" p. 266, published by Baifukan
- \_\_\_\_\_ 2. Soden et al., "Identifying Defects in Deep-Submicron CMOS Ics", September 1996, pp. 66-71, IEEE SPECTRUM
- \_\_\_\_\_ 3. Mizuno et al., "A Lean-Power Gigascale LSI Using Hierarchical VBB Routing Scheme with Frequency Adaptive VT CMOS", 1997, pp. 95-96, Symposium on VLS Circuits Digest of Technical Papers

EXAMINER

DATE CONSIDERED

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